ARTEMIS JOINT UNDERTAKING
The public private partnership for R&D in the field of Artemis

SHIELD
PILOT

WP3: SPD Node

Review September 2011

Przemysław Osocha (SESM), major contributions from:
MAS, CWIN, ETH, SESM, CS, AS, ATHENA,

ARTEMIS Call 2009 – SP6100204

WP3 Introduction – Work Package subject & objectives

Subject:

- Basic components of the SPD Pervasive System
- Intelligent ES Nodes of increasing complexity:
  - nano node,
  - micro/personal node,
  - power node.

Objectives:

- Provide SPD intrinsic capabilities at node layer
- Create an Intelligent ES HW/SW Platform

WP3 Introduction – Tasks

- WP 3 – SPD Node
  - ✓ **WP leader: SESM**

- Task 3.1 - Nano, Micro/Personal node
  - ✓ **Task leader: THYIA**,
  - ✓ Task partners: AS, CS, CWIN, MAS, (ISD withdrew)
- Task 3.2 - Power node
  - ✓ **Task leader: ETH**,
  - ✓ Task partners: SESM, AS, CWIN
- Task 3.3 - Dependable self-x and cryptographic technologies
  - ✓ **Task leader: AS**,
  - ✓ Task partners: CS, ATHENA, THYIA

WP3 Introduction – Deliverables

Internal

- D3.1 - SPD node technologies prototypes
  - ✓ Output of WP3 (Tasks: 3.1, 3.2 and 3.3)
  - ✓ **SESM**, AS, ATHENA, CS, CWIN, ETH, MAS, THYIA, (ISD)
  - ✓ Month M15

Public

- D3.2 - SPD nano, micro/personal node technologies prototype report
  - ✓ Output of Tasks: 3.1
  - ✓ **THYIA**, AS, CS, CWIN, MAS, (ISD)
  - ✓ Month M16

- D3.3 - SPD power node technologies prototype report
  - ✓ Output of 3.2
  - ✓ **ETH**, SESM, AS, CWIN
  - ✓ Month M17

- D3.4 - SPD self-x and cryptographic technologies prototype report
  - ✓ Output of Tasks 3.3
  - ✓ **AS**, CS, ATHENA, THYIA
  - ✓ Month M16

WP3 Status – Deliverables

Internal

- D3.1 SPD node technologies prototypes
  - Delivered, but under continuous enhancements

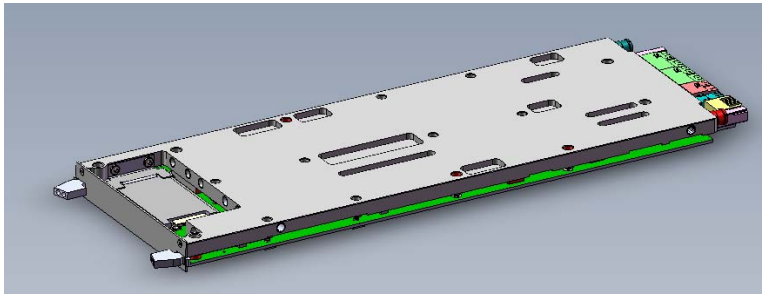
Public

- D3.2 SPD nano, micro/personal node technologies prototype report
  - Draft,ToC available at bscw server, works assigned
- D3.3 SPD power node technologies prototype report
  - Draft,ToC available at bscw server, works assigned
- D3.4 SPD self-x and cryptographic technologies prototype report
  - Draft, 70% ready, available at bscw server

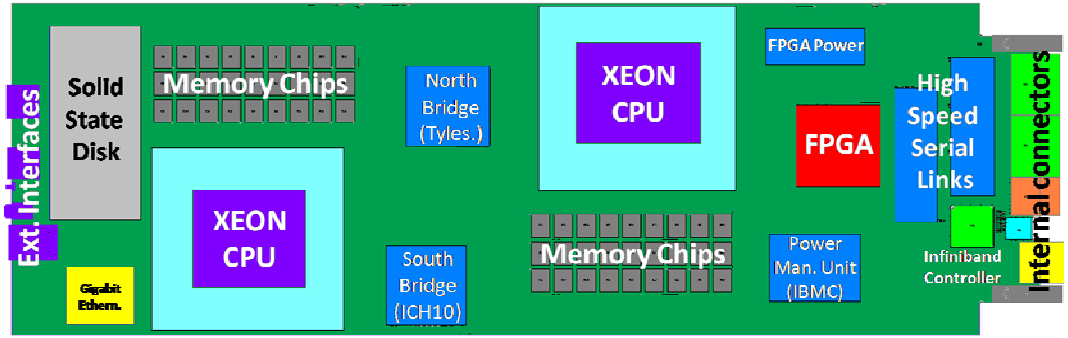
Rugged High Performance Computing Node (ETH)

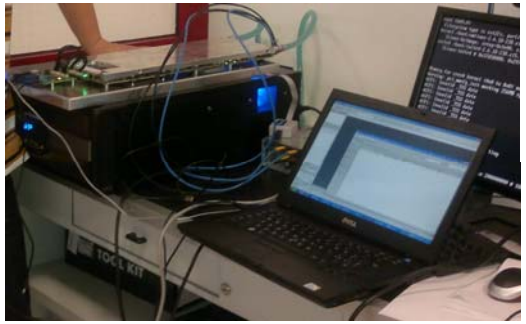
- The Power Node is a high performance embedded PC and the position of components is crucial to ensure the required performances (computing power, throughput, heat dissipation, etc.):
  - CPU positioning to maximize performance and parallelism;
  - Memory/CPU close coupling;
  - Connector positioning to ensure easy composability;
  - Distribution of components to optimize heat dissipation;
  - PCB power aware design;
  - First analysis of the cold-plate heating system.

Results described in **D2.3.1, D.3.1**, and future **D3.3**



•The Power Node is an Intel based platform with 2 Nehalem/Wesmare Xeon dual-processor.
•It is an open node of pShield and nShield platform because it contains an high speed FPGA (Altera Stratix IV) that allows the user to create its own customized hardware.



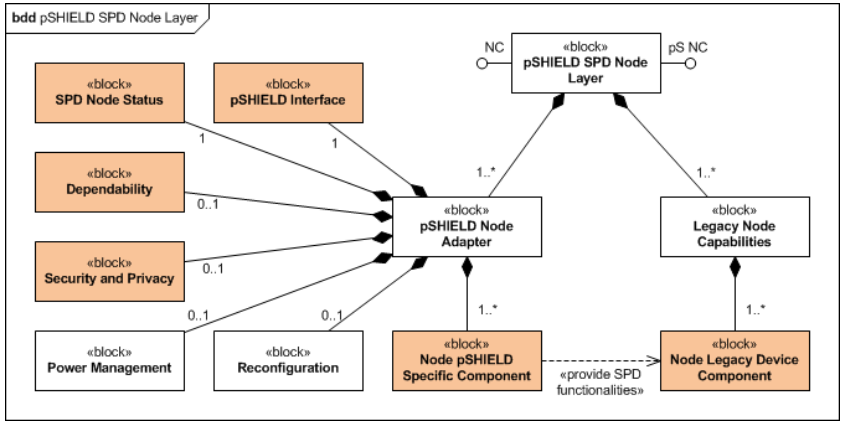


pSHIELD SPD Node Layer Conceptual Model (SESM)

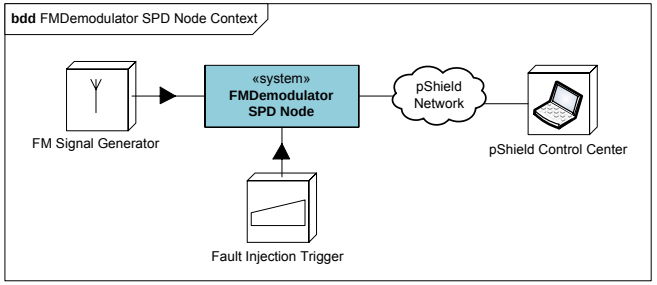
•*Development of Node Requirements that follow TA. Results in **D2.1.1** chapter 8 "Node Requirements and Specifications"*

• *Design of generic conceptual model of a pSHIELD node for all node types, which can be implemented in different architectures, providing different functionalities, different SPD compliance levels and different services, depending on the type of node and application field.*
*Three node types share the same conceptual model, enabling a seamless composability. Contributed to **D2.3.1** (Node section) and to new deliverable **M0.1**.*

•*The first version of pSHIELD SPD FPGA Power Node prototype was developed. Results in **D3.1**, final report will be in **D3.3**.*



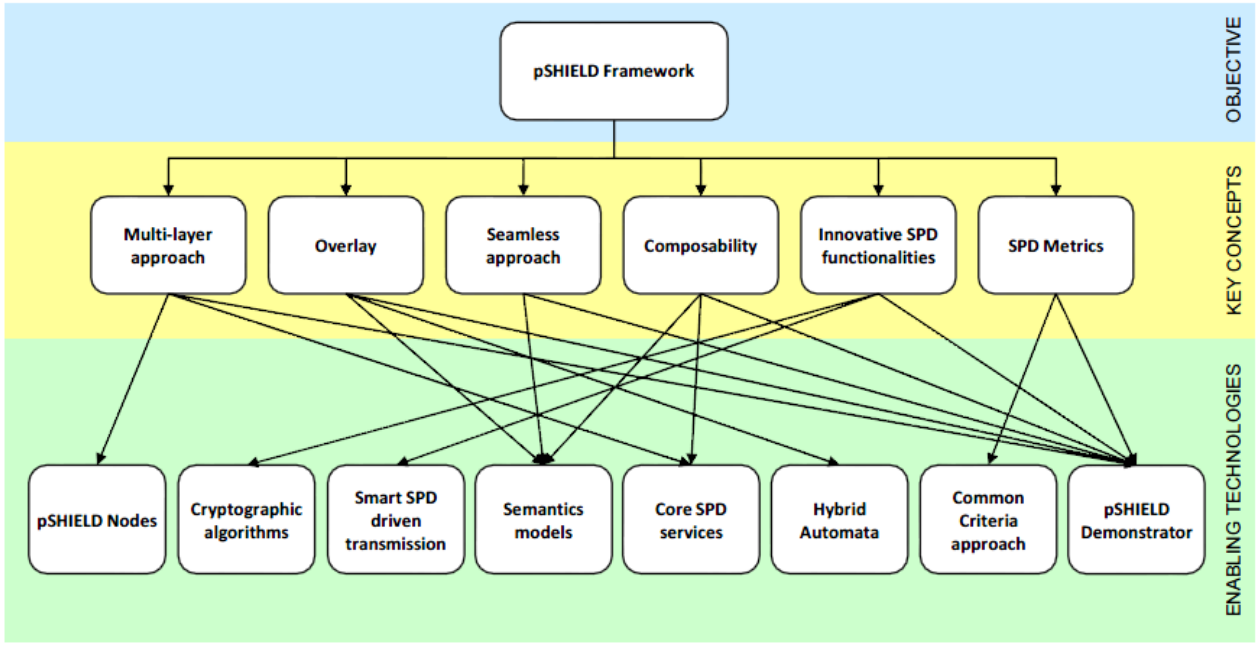
pSHIELD SPD Node Layer Conceptual Model



Node Layer Application Scenario

Hardware and software crypto technologies (CS, ATHENA)
Cryptography for embedded devices

- Cryptography algorithms made a fundamental contribution for the provision of different systems security, inside the pSHIELD enabling technologies.

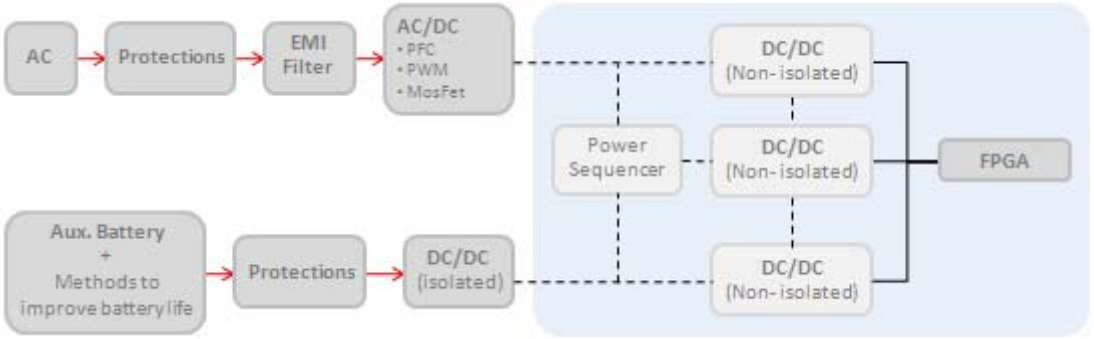


The main enabling technologies and their main relation

Results presented in **D3.1** and **D3.4**

Dependable power supply (AS)

- *The power supply design for an ES is one of the critical points in the design process, due to the requirements are more restrictive as time goes by.*



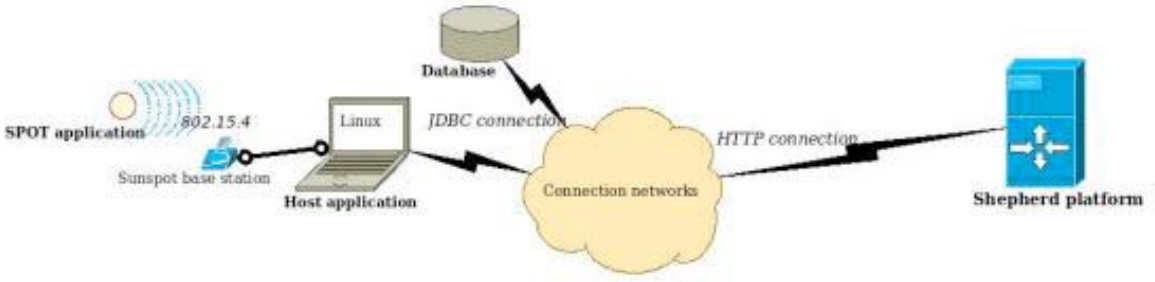
Power supply components - General design (power node)

To protect the systems against external attacks, it is important to design the properly power supply protections. These will focus on three key points:

- *Study how to provide a continuous power supply source, without any cut in time or, at least, how to keep the system running during a period of time long enough to solve the problem with the main source or to send a warning to alert the person in charge.*
- *Design the appropriate protections to avoid system damages, including different operation modes to plug or unplug critical and non-critical sections of the nodes.*
- *Monitor the power consumption*

*Results are presented in **D3.1**, and future **D3.2, D3.3, D3.4***

Nano and power nodes integration (CWIN, MAS)



System overview, communication between Sun SPOT sensors and its base station, and between the ES and the Shepherd Platform.

Integration aspects of micro, power and possibly personal node with the demonstrator.

- Micro Node – Sun SPOT Sensor Platform
- Power Node – VIA Embedded Board
- *Integration with Telenor Shepherd® Platform*
- *Connectivity with Shepherd® Platform*

*Results are presented in **D3.1**, and future **D3.2** and **D3.3.***

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SHIELD

PILOT

WP3 Status

Leader : SESM

ARTEMIS Call 2009 – SP6100204

SESM A Finmeccanica Company · Thyia Technologies · Sapienza Università di Roma · Hellenic Aerospace Industry · EuroTech · Movation · Critical Software · DIBE · Selex Elsag A Finmeccanica Company · I.S.I. Industrial Systems Institute · Mondragon Unibertsitatea · AnsaldoSTS A Finmeccanica Company · tecnalia Inspiring Business · CWI · AC · Tecnologie nelle Reti e nei Sistemi T.R.S. SpA

WP3 Status – Meetings and conferences

- **Frequent PhCs assure collaboration and information exchange**
- WP3 Phone Conferences
  - 2010.12.14 PhC WP3
  - 2011.02.25 PhC WP3
  - Participation in pre/post Mid-term works
  - 2011.04.18 PhC WP3
  - 2011.05.24 PhC WP3
  - 2011.06.21 PhC WP3
  - Participation in Rome Consortium Meeting
  - 2011.09.09 PhC WP3
- Interactive MoMs available pSHIELD Wiki and also at repository bscw server
- WP3 Tasks PhCs performed on regular basis